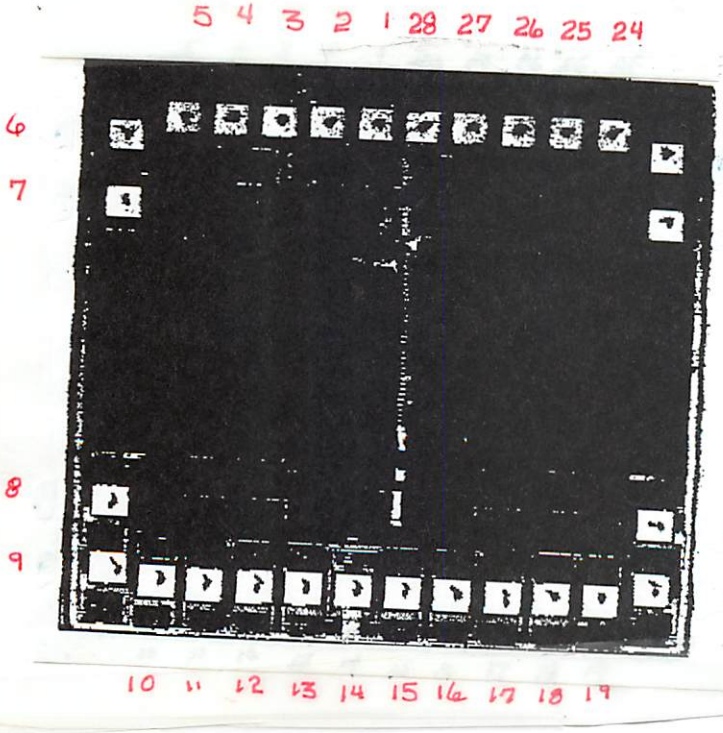
ISO9002 Certified SCI Quality System

Sierra Components, Inc.

924 Incline Way •Suite F • Incline Village, Nevada 89451
Phone: 775.831.1241 Fax: 775.831.3021

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD FUNCTIONS

1)	VCC	10)	A0	19)	O7	28)	VCC
2)	A12	11)	O0	20)	CE	29)	
3)	A7	12)	O1	21)	A10	30)	
4)	A6	13)	O2	22)	OE	31)	
5)	A5	14)	VSS	23)	A11	32)	
6)	A4	15)	O3	24)	A9	33)	
7)	A3	16)	O4	25)	A8	34)	
8)	A2	17)	O5	26)	VPP	35)	
9)	A1	18)	O6	27)	PGM	36)	

Topside Met:
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY:	**DIE SIZE (Mils): 102 X 111**	**DATE: 3/3/00**
MFG: AMD	**THICKNESS:**	**P/N: AM27C64**